



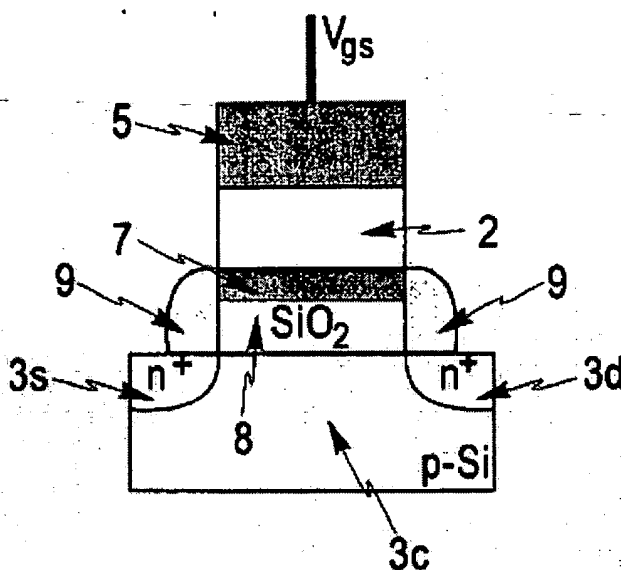
BEST AVAILABLE COPY**Ferroelectric memory transistor with resistively couple floating gate****Publication number:** CN1211827**Publication date:** 1999-03-24**Inventor:** BLACK CHARLES T (US);
WELSER JEFFREY J (US)**Applicant:** IBM (US)**Classification:****- international:** *G11C11/22; H01L21/8246;
H01L21/8247; H01L27/10;
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G11C11/22; H01L21/70;
H01L27/10; H01L27/105;
H01L29/66; (IPC1-7): H01L29/786***- european:** H01L29/78K; H01L29/788B4**Application number:** CN19981017294 19980814**Priority number(s):** US19970929878 19970915**Also published as:** US6069381 (A1) JP11135737 (A) CN1147001C (C)**Report a data error here**

Abstract not available for CN1211827

Abstract of corresponding document: **US6069381**

The present invention proposes a new type of single-transistor memory device, which stores information using the polarization of a ferroelectric material. The device is a floating-gate FET, with a ferroelectric material positioned between the gate and the floating gate, and a resistance, preferably in the form of a thin SiO₂ dielectric between the floating gate and the transistor channel. Unlike previous designs, in this device the floating gate is both capacitively and

resistively coupled to the transistor channel, which enables the device to be both read and written using low voltages. This device offers significant advantages for operation at low voltages and at high speeds, for repeated cycling of over 10^{10} times, since device durability is limited by the ferroelectric endurance rather than oxide breakdown, and for integration at gigabit densities.



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